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CPE221

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Homework 8

**9.92**

**64 bytes x 1 word / 4 bytes x 1 line / 2 words x 1 set / 2 lines = 4 set**

**4 sets**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Set | Tag | Data | Tag | Data |
| 0 | 001,010 | M[20…23], M[40…43] | 100 | M[80…83] |
| 1 |  |  | 001 | M[24…27] |
| 2 | 001 | M[28..2B] | 010 | M[48..4B] |
| 3 | 000,001 | M[0C..0F], M[2C..2F] | 010 | M[4C..4F] |
| 4 | 001 | M[30..33] |  |  |
| 5 |  |  | 001 | M[34..37] |
| 6 | 001 | M[38..3B] |  |  |
| 7 | 001 | M[3C..3F] | 010 | M[5C..5F] |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 48 010 010 00 Miss | 5C 010 111 00 Miss | 22 001 000 10 Hit | 30 001 100 00 Miss | 24 001 001 00 Hit |
| 0C 000 011 00 Miss | 3A 001 110 10 Miss | 24 001 001 00 Miss | 34 001 101 00 Miss | 28 001 010 00 Miss |
| 48 010 010 00 Hit | 20 001 000 00 Miss | 81 100 000 01 Miss | 27 001 001 11 Hit | 2C 001 011 00 Miss |
| 4C 010 011 00 Miss | 21 001 000 01 Hit | 49 010 010 01 Hit | 3E 001 111 10 Miss | 40 010 000 00 Miss |

**9.97**

**a.)** What is the address format for a direct-mapped cache with a block size of 32 words?

32KB x (1 word / 8 bytes) x (1 line x 32 words) x ( 1set / 1 line) = **8 bits = block Offset**

Block inside cache: (32x1024)/(32x5) = log128 = **7 index bits**

Tag bits = 24-(7+8) = **9 tag bits**

**- Byte offset = 3, Tag Bits = 9, Index Bits = 7, Block Offset = 8.**

**b.)** What is the address format for a fully associative cache with a line size of 16 words

Block size = 16 words, 16x8 = 128 bytes. Block offset = log128 = 7 bits

Tag bits = 24 – 7 = 17, index bits = 0.

**Byte Offset = 3, Tag Bits = 17, Set Index = 0. Block Offset = 7**

**c.)** What is the address format for a four-way set-associative cache with a line size of 8 words?

Block size = 8 words, 8 x 8 = 64 bytes.

Block offset = 6 bits

Block inside cache = (2^15 / 2^6) = 512

Set inside cache = 512 / 8 = 64

Set bits = 6 bits

Tag = 24-12 = **Byte Offset = 3, Tag Bits = 12, Set Index = 6, Block Offset = 6**